

What is claimed is:

1. A method of manufacturing semiconductor devices, comprising:

5 forming element isolation regions in a semiconductor substrate;

 forming a gate insulation film in an element region surrounded by said element isolation regions;

10 forming an impurity doped metal silicide film on said gate insulation film;

 irradiating energy beams to heat said silicide film;

 forming a gate electrode film by patterning said silicide film; and

15 forming source and drain regions by doping an impurity into said element region by using at least said gate electrode film as a mask.

2. A method of manufacturing semiconductor devices according to Claim 1, further comprising;

20 forming extension regions by doping an impurity into a region surrounding said element region by using said gate electrode film as a mask, wherein said forming of said extension regions is carried out between said forming of said gate electrode film and said forming of said source and drain regions; and

25 forming a sidewall insulation film on a sidewall of said gate insulation film.

3. A method of manufacturing semiconductor devices,
comprising:

forming element isolation regions in a semiconductor
5 substrate;

forming a dummy gate insulation film in an element
region surrounded by said element isolation regions;

forming a dummy gate electrode film on said dummy gate
insulation film;

10 patterning said dummy gate electrode film to form a
dummy gate electrode;

doping an impurity to form extension regions surrounding
said element region by using said dummy gate electrode as a mask;

forming a sidewall insulation film on a side surface of
15 said dummy gate electrode; forming source and drain regions by
doping an impurity into said element region by using said dummy
gate electrode provided with said sidewall insulation as a mask;

covering said source and drain regions and said dummy
gate with an interlayer insulation film;

20 making said interlayer insulation film substantially even
to expose said dummy gate electrode;

eliminating said dummy gate electrode and said dummy
gate insulation film to define a space;

forming a gate insulation film in said space on said
25 semiconductor substrate;

forming an impurity doped metal silicide film on said gate

insulation film; and

irradiating energy beams to heat said silicide film.

4. A method of manufacturing semiconductor devices
5 according to Claim 1 wherein said impurity doped silicide film
contains an impurity to provide said impurity doped silicide film
with an electrically conductive type.

5. A method of manufacturing semiconductor devices
10 according to Claim 3 wherein said impurity doped silicide film
contains an impurity to provide said impurity doped silicide film
with an electrically conductive type.

6. A method of manufacturing semiconductor devices,
15 comprising:

forming element isolation regions in a semiconductor
substrate;

forming first conductive type and second conductive type
wells for making first conductive type and second conductive type
20 metal insulator field effect transistor regions surrounded by said
element isolation regions, respectively;

forming gate insulation films on said first conductive type
and second conductive type metal insulator gate field effect
transistor regions;

25 forming silicide films on said gate insulation films;

doping a first conductive type impurity into said silicide

film on said first conductive type metal insulator gate field effect transistor region;

irradiating energy beams to heat said silicide film into which said first conductive type impurity is doped;

5 patterning said silicide films to form gate electrode films;
and

doping first conductive type and second conductive type impurities into said first conductive type and second conductive type metal insulator gate field effect transistor regions to form
10 source and drain regions by using at least said gate electrode films as a mask, respectively.

7. A method of manufacturing semiconductor devices according to Claim 6, further comprising;

15 forming extension regions by doping an impurity into a region surrounding said element region by using said gate electrode film as a mask, wherein said forming of said extension regions is carried out between said forming of said gate electrode film and said forming of said source and drain regions; and

20 forming a sidewall insulation film on a sidewall of said gate insulation film.

8. A method of manufacturing semiconductor devices according to Claim 6, further comprising:

25 doping a second conductive type impurity into said silicide film of said second conductive type metal insulator gate

field effect transistor region between said doping of said first
conductive type impurity into said silicide film of said first
conductive type metal insulator field effect transistor region and
said irradiating of said energy beams to heat said silicide film into
5 which said second conductive type impurity is doped.

9. A method of manufacturing semiconductor devices
comprising:

forming element isolation regions in a semiconductor
10 substrate;

forming first conductive type and second conductive type
well regions surrounded by said element isolation regions to make
second conductive type and first conductive type metal insulator
gate field effect transistor regions, respectively;

15 forming dummy gate insulation films in said first
conductive type and second conductive type metal insulator gate
field effect transistor regions;

forming dummy gate electrode films on said dummy gate
insulation films;

20 patterning said dummy gate electrode films to make
dummy gate electrodes;

doping first conductive type and second conductive type
impurities into said first conductive type and second conductive
type metal insulator field effect transistors, respectively, to form
25 extension regions by using said dummy gate electrode as a mask;

forming a sidewall insulation film on a sidewall of said

dummy gate electrode;

doping first conductive type and second conductive type impurities into said first conductive type and second conductive type metal insulator field effect transistors, respectively, to form
5 source and drain regions by using said dummy gate electrode provided with said sidewall insulation film as a mask;

covering said source and drain regions and said dummy gate with an interlayer insulation film;

making said interlayer insulation film substantially even
10 to expose said dummy gate electrode;

eliminating said dummy gate electrode and said dummy gate insulation films to define a space;

forming a gate insulation film in said space on said semiconductor substrate;

15 forming a silicide film on said gate insulation film;

doping a first conductive type impurity into said silicide in said first conductive type metal insulator field effect transistor region; and

irradiating energy beams to heat said silicide into which
20 said first conductive type impurity is doped.

10. A method of manufacturing semiconductor devices according to Claim 8, further comprising;

doping a second conductive type impurity into said
25 silicide film of said second conductive type metal insulator gate field effect transistor region between said doping of said first

conductive type impurity into said silicide film of said first
conductive type metal insulator gate field effect transistor region
and said irradiating of said energy beams to heat said silicide film
into which said second conductive type impurity is doped.

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11. A method of manufacturing semiconductor devices
according to Claim 1, further comprising;

forming a metal or silicide layer on said source and drain
regions after said forming of said source and drain is carried out.

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12. A method of manufacturing semiconductor devices
according to Claim 3, further comprising;

forming a metal or silicide layer on said source and drain
regions after said forming of said source and drain is carried out.

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13. A method of manufacturing semiconductor devices
according to Claim 6, further comprising;

forming a metal or silicide layer on said source and drain
regions after said forming of said source and drain is carried out.

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14. A method of manufacturing semiconductor devices
according to Claim 9, further comprising;

forming a metal or silicide layer on said source and drain
regions after said forming of said source and drain is carried out.

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15. A method of manufacturing semiconductor devices

according to Claim 1, wherein said energy beams are incoherent light.

16. A method of manufacturing semiconductor devices
5 according to Claim 3, wherein said energy beams are incoherent light.

17. A method of manufacturing semiconductor devices
according to Claim 6, wherein said energy beams are incoherent
10 light.

18. A method of manufacturing semiconductor devices
according to Claim 9, wherein said energy beams are incoherent
light.

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